

IN THE U.S. PATENT AND TRADEMARK OFFICE

Applicant: Tetsuya AKAMATSU et al.
Appl. No.: NEW Group:
Filed: April 22, 2004 Examiner:
For: POWER-ON RESET CIRCUIT

INFORMATION DISCLOSURE STATEMENT
(SUBMISSION CONCURRENT WITH THE
FILING OF A NEW PATENT APPLICATION)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

April 22, 2004

Sir:

Pursuant to 37 C.F.R. §§ 1.97 and 1.98, applicant(s) hereby submit(s) an Information Disclosure Statement for consideration by the Examiner.

I. LIST OF PATENTS, PUBLICATIONS OR OTHER INFORMATION

The patents, publications, or other information submitted for consideration by the Office are listed on PTO-1449, attached hereto.

II. COPIES

- a. ☐ This application was filed before June 30, 2003. Accordingly, submitted herewith is a legible copy of (i) each U.S. and foreign patent; (ii) each publication or that portion which caused it to be listed; and (iii) all other information or that portion which caused it to be listed.
- b. ☒ This application was filed on or after June 30, 2003. Accordingly, copies of cited US patents and patent application publications therefore are not included. Copies of foreign patent documents and non-patent literature are included.

- c. ☐ This application is a National Phase of a PCT application. Some or all of the documents listed on the PTO-1449 are not enclosed because they were cited in the International Search Report and copies should be forwarded from the International Search Authority. If copies are needed, please contact the undersigned.

III. CONCISE EXPLANATION OF THE RELEVANCE

(check at least one box)

- a. ☐ **DOCUMENTS IN THE ENGLISH LANGUAGE**

The patents, publications, or other information listed on the attached PTO 1449 are in the English language and therefore, do not require a statement of relevancy.

- b. ☒ **DOCUMENTS NOT IN THE ENGLISH LANGUAGE**

A concise explanation of the relevance of all patents, publications, or other information listed that is not in the English language is as follows:

An English language Partial Translation is provided for all documents not listed in the English language, thereby satisfying the relevancy requirements.

- c. ☐ **ENGLISH LANGUAGE SEARCH REPORT**

An English language version of the search report or action that indicates the degree of relevance found by the foreign office is attached, thereby satisfying the requirement for a concise explanation. See MPEP 609(III) (A) (3).

- d. ☐ **OTHER**

The following additional information is provided for the Examiner's consideration.

FEES

This Information Disclosure Statement is being filed concurrently with the filing of a new patent application; therefore, no fee is required.

If the Examiner has any questions concerning this IDS, he/she is requested to contact the undersigned. If it is determined that this IDS has been filed under the wrong rule, the PTO is requested to consider this IDS under the proper rule and charge the appropriate fee to Deposit Account No. 02-2448.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. § 1.16 or under § 1.17; particularly, extension of time fees.

Respectfully submitted,

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Attachment(s) : ☒ Form PTO-1449(s)
☒ Documents
☐ Foreign Search Report
☐ Fee
☐ Other: _____

(Rev. 02/12/2004)

IDS

Please file the IDS related documents of the above referenced application, according to the information provided below:

- (1) A list of information:
- | | | | | |
|-------------------------------|----------|------------|--------|-------------|
| 1. | Japanese | Unexamined | Patent | Application |
| Publication No. Hei 06-196989 | | | | |
| 2. | Japanese | Unexamined | Patent | Application |
| Publication No. Hei 11-68539 | | | | |

(2) Legible copies of the above-listed publications are attached.

(3) A concise explanation of the relevance about the above-listed publications is incorporated in the applicant's specification.

(4) A copy of the translation of the above-listed publication 1 is attached. The partial translation is one for its abstract provided by the Japan Patent Office.

The partial translation of the above-listed 1 publication:

1. Japanese Unexamined Patent Application Publication No. Hei 06-196989

Abstract:

PURPOSE: To generate a prescribed reset pulse independently of the characteristics of power supply voltage by ending an input voltage at a previously set voltage by a voltage control means when the input voltage exceeds the set voltage, and when the input voltage is dropped less than the set voltage, outputting the input voltage.

CONSTITUTION: When power supply voltage VDD is gradually risen a reset pulse having time width determined by the voltage rising characteristics of the power supply VDD, the threshold value of a transistor P1 and the rotational threshold value of an inverter 11 is outputted and the system is reset by the pulse. When the dimensions of transistors (TRs) ND, N1 comprising a voltage control part 4 are properly designed, a required voltage can be obtained on a control point V1 to be the output of the voltage control part 4, so that power supply voltage for outputting a reset pulse to a relating system can be optionally set up.

The partial translation of the above-listed 2 publication:

1. Japanese Unexamined Patent Application Publication No. Hei 11-68539

Abstract:

PROBLEM TO BE SOLVED: To provide power on reset circuit with a simple structure that surely forms one-shot pulse, regardless of the start up speed of a power source voltage.

SOLUTION: When a power source potential Vcc rises up to a specified level through the application of a power source, PMOSs 61 to 63 in a power source voltage detection circuit 60 are connected, the voltage of a node N60 is set, and a PMOS 71 is turned on. Thus, a capacitor 73 is charged, and the voltage of a node N 70 rises. When the voltage of the node N70 rises and exceeds a threshold of an inverter 75, a logical level outputted by this inverter 75 changes from 'H' into 'L'. When the power source potential Vcc rises further, the PMOS 61 is turned off and a subsequent current consumption becomes 0.

